Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for providing variable output drive capability, comprising:

generating a two-bit signal representative of the relative strength of an n-channel transistor and a p-channel transistor in an output device; and

controlling with a plurality of switches the number of output pre-driver stages that are active on a first data path and on a second data path in response to said two-bit signal, wherein at least a first pair of said output pre-driver stages is controlled by one-bit of said two-bit signal and at least a second pair of said output pre-driver stages is controlled by the other bit of said two-bit signal, and wherein one output pre-driver stage of each pair is connected to said first data path and another of each pair of output pre-driver stages is connected to said second data path.

2. (Original) The method of claim 1 wherein said controlling is further in response to the relative size of said output pre-driver stages.

3. (Original) A method, comprising:

generating a two-bit signal representative of the relative strength of an n-channel transistor and a p-channel transistor in an output device;

enabling with a plurality of switches certain output stages in a pre-driver in response to said signal, wherein said pre-driver includes a first data path and a second data path and wherein said pre-driver produces a variable output drive capability, and wherein at least a pair of said certain output stages is enabled in response to said signal, said pair having an output stage connected to said first data path and another output stage connected to said second data path; and

inputting a high and a low data signal to the output device through said pre-driver.

4. (Original) The method of claim 3 wherein said enabling is further in response to the relative size of said output stages.

5. (Original) The method of claim 3 wherein said enabling step reduces skew in the data output by the output device.

6. (Original) A pre-driver providing variable output drive capability, comprising:

a first data path having a plurality of pre-driver output transistors;

a second data path having a plurality of pre-driver output transistors; and

a plurality of switches, each switch for enabling a pair of said plurality of pre-driver output transistors in response to signals indicative of the strength of driver output transistors in an output device, wherein one of said pair of pre-driver output transistors is connected to said first data path and another of said pair of pre-driver output transistors is connected to said second data path.

7. (Original) The pre-driver of claim 6 wherein at least one of said plurality of pre-driver output transistors is sized differently relative to another of said plurality of pre-driver output transistors.

8. (Original) A portion of a data path, comprising:

an output driver responsive to a data signal; and

a pre-driver providing variable output drive capability, comprising:

a first pre-driver data path having a plurality of output transistors;

a second pre-driver data path having a plurality of output transistors; and

a plurality of switches, each switch for enabling a pair of said plurality of pre-driver output transistors in response to signals indicative of the strength of output transistors in said output driver, wherein one of said pair of output transistors is connected to said first pre-driver data path and another of said pair of output transistors is connected to said second pre-driver data path, said pre-driver for providing said data signal to said output driver.

9. (Original) The portion of a data path of claim 8 wherein at least one of said plurality of pre-driver output transistors of said pre-driver is sized differently relative to another of said plurality of pre-driver output transistors of said pre-driver.

10. (Original) A memory device, comprising:

a plurality of memory cells arranged in an array of rows and columns;

a plurality of devices for identifying cells within said array;

a plurality of pads;

a data path connecting said plurality of pads and said array, said data path including

an output driver responsive to a data signal; and

a pre-driver providing variable output drive capability, comprising:

a first pre-driver data path having a plurality of output transistors;

a second pre-driver data path having a plurality of output transistors; and

a plurality of switches, each switch for enabling a pair of said plurality of pre-driver output transistors in response to signals indicative of the strength of output transistors in said output driver, wherein one of said pair of output transistors is connected to said first pre-driver data path and another of said pair of output transistors is connected to said second pre-driver data path, said pre-driver for providing said data signal to said output driver.

11. (Original) The memory device of claim 10 wherein at least one of said plurality of pre-driver output transistors within said data path is sized differently relative to another of said plurality of pre-driver output transistors within said data path.

12. (Original) A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus;

an output device coupled to the processor through the processor bus;

a memory device coupled to the processor bus, the memory device comprising:

a plurality of memory cells arranged in an array of rows and columns;

a plurality of devices for identifying cells within said array;

a plurality of pads;

a data path connecting said plurality of pads and said array, said data path including:

an output driver responsive to a data signal; and

a pre-driver providing variable output drive capability, comprising:

a first pre-driver data path having a plurality of pre-driver output transistors;

a second pre-driver data path having a plurality of pre-driver output transistors; and

a plurality of switches, each switch for enabling a pair of said plurality of pre-driver output transistors in response to signals indicative of the strength of output transistors in said output driver, wherein one of said pair of pre-driver output transistors is connected to said first pre-driver data path and another of said pair of output transistors is connected to said second pre-driver data path, said pre-driver for providing said data signal to said output driver.

13. (Original) The computer system of claim 12 wherein at least one of said plurality of pre-driver output transistors within said data path is sized differently relative to another of said plurality of pre-driver output transistors within said data path.